**cProgramming Project #1**

***Due Date: 10/20, Wed., 11:59 p.m. Please submit via Blackboard. Late submissions are accepted till 10/25, 11:59. p.m., with 10% penalty each day. No submissions accepted after 10/25, Monday, 11:59 p.m.***

***Please name your submission file starting with “LastName\_FirstName\_PP1”.***

Please develop a RISC-V code fragmentcalled extract\_fields procedure that takes two arguments. The first argument (a0) is a given 32-bit R-type instruction. The second argument (a1) is an integer number with one of the following values: 0, or 1, or 2. The procedure performs the following functionality:

* if the second argument is 0, the procedure returns the opcode field of the given instruction in the first argument (a0);
* if the second argument is 1, the procedure returns the rd field of the given instruction;
* if the second argument is 2, the procedure returns the rs1 field of the given instruction.

Please either use the FreedomStudio/QEMU simulator [1] or the BRISCV simulator [2] to run and verify the result with two given instructions: 0x015A04B3 and 0x00578833.

Please provide your RISC-V code fragment. In addition, please either provide a recorded ~5-minute video (with audio) to demo how you either use the FreedomStudio/QEMU simulator or the BRISCV simulator to verify the result with two given instructions: 0x015A04B3 and 0x00578833, or request a ~5-minute demo with our TA before the end of October. If you provide a recorded video, please provide the URL to your video (you can either use OneDrive, or Google Drive, or Dropbox, or another solution to host your video).

Lecture 14 provides more details about this programming project.

[1] FreedomStudio/QEMU: <https://github.com/sifive/freedom-studio/releases/tag/v2020.06.3>

[2] BRISCV simulator: <https://ascslab.org/research/briscv/simulator/simulator.html>

THE END.

**Instruction:** 0x015A04B3

0000 0001 0101 1010 0000 0100 1011 0011

Opcode: 011 0011 OR 0x33

Rd: 0100 1 OR 0x9

Rs1: 1010 0 OR 0x14

**Instruction:** 0x00578833

0000 0000 0101 0111 1000 1000 0011 0011

Opcode: 011 0011 OR 0x33

Rd: 1000 0 OR 0x10

Rs1: 0111 1 OR 0xF